A PROTOTYPE DESIGN APPROACH FOR LIGHTNING DIRECT STRIKE TEST FACILITY

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Abstract

After evaluating the engineering requirements, costs, and performance simulations of various Capacitive and Inductive Energy Storage Pulsed Power Systems concepts, we have settled on some concise design capable of generating peak current pulse of 200 KA, with 6.36 μs rise-time, and d*i*/dt of 139 kA/μs for the Lightning Direct Strike Test Facility at White Sands Missile Range, NM. Unlike the recently refurbished Sandia Lightning Simulator which uses YAG laser induced spark-gap triggering, our design relies on high-power diodes as crowbar switch that automatically shunts the peak current pulse at the desired point in time, and for the desired decay through RL sub-circuitry. Also discussed herein are the various aspects of engineering, performance, and reliability of the diodes, the crucial switching components, and evaluation of the key parameters, such as dynamic resistance during forward recovery transient, and high d*i*/dt impact on modulation conductivity, all of which will eventually be resolved using advanced diffusion physics simulations.

I. INTRODUCTION

The current existing Lightning Test Facility (LTF) for indirect strike testing at White Sands Missile Range (WSMR) can not generate the peak current specified in MIL-STD-464A while the pulse shape of erratic behaviors has the rise time much faster in nano-second range. These problems exist since it was secured by WSMR with inconsistent replacements of LC design parameters from original vendor Thiokol designed for NASA. As original design documents were disappeared for long, we had reevaluated the new engineering designs, system requirements and associated costs for Direct Strike LTF (DSLTF) to test mostly the small scale critical weaponry components like Explosive Electronic Devices (EED) for Electromagnetic Compatibility (EMC) issues.

In this paper, only the major concerns of the conceptual design approaches and relevant system engineering criteria for the prototype pulse generator are discussed. Other important system components like Transmission Line (TL), Spark Gap breakdown and topics of design factors such as ground impedance / ground loop effects, diagnostic instrumentations and relevant electromagnetic interference (EMI) are excluded here for the future.

[†]

II. Prototype Conceptual Design Approaches

The design considerations are exhausted with various concepts of Capacitive / Inductive Energy Storage Pulsed Power Systems (CESPP/IESPP) as shown in Table 1 of last page. The conventional gigantic CESPP MV-scale Marx generator design as adopted in many high voltage pulsed power systems is excluded simply from design options for its tremendous cost over millions of dollars. This is because that it usually consisted of a large number of capacitors of low capacitances in series to build up bank voltage to MV or higher but adversely reducing its erected capacitance, thus require several parallel banks of series capacitors to make enough desired system capacitance, and specialty to submerge the matrix capacitors in oil to avoid over-voltage breakdown. Besides, to synthesize relevant performance of the conventional RLC circuit designs with peaking capacitors, Lapalce transform, an unavailable analytical math tool, only can solve simple coupled linear circuitry.

The IESPP Opening Switch (OS) technologies are very attractive as considering energy efficient and engineering features. New innovative OS technologies like Solid State Switch, Photoconductive and Pseudospark Switch, explosive wire OS etc. are still under development and mostly require some extensive R&D to comply with the pulse criteria, particularly the charge action for direct strike. As bounded by stringent budget unable to afford R&D cost, these OS are rejected in the design options. While High Power Consulting's exploding foil fuses OS, full interruption infinite off resistance, cost very little but required the furnishings of OSs at some extraordinary maintainability as maximum dwell break time between consecutive single-strokes is mandatory for repeated numerous tests within each mission schedule.

The first several candidates for DSLTF system designs are thus left with CESPP - Redstone DSLTF simulator based on conventional RLC circuitry; Sandia Lightning Simulator (SLS) and British ABE LSS with crowbar switch, both designs employ no peaking capacitors.

The CESPP RLC Circuitry system design similar to SLS is finally adopted but use high-power diodes as crowbar switch[*], as suggested by Dr. Charles R. McClenahan[2]. This automatic triggering has a big

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14. ABSTRACT
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15. SUBJECT TERMS

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advantage over SLS's YAG lasers electronically controlled crowbar switch.

**One noteworthy innovation super-GTO switch[4] with promising features, developed for ARL by Dr. Vic Temple at Silicon Power, Inc., was declined for its higher cost under development and requiring extra special triggering device to shunt the peak current.*

Furthermore, for comparison the refurbished SLS has two Marx capacitor banks with an erected capacitance of 325 nF. When fired, the banks erect to approximately 1 MV[1], with stored energy 176 kJ. Hence, the banks have to be submerged in a huge transformer oil tank for high voltage insulation. WSMR new DSLTF design only requires one two-capacitor bank with an erected capacitance of 25 µF with erected 32 kV, thus, no need for oil insulation. It has fractional stored energy 35.50 kJ due to very low effective voltage from generator, or actually resulting from very low system inductance[5.A].

III. System Design Criteria / Methodologies

The principles for WSMR new DSLTF designs are based on compact portability testing requirement for size fitted in a normal 40-foot shipping conex. As mission requiring explosive devices like EED under direct strike test, a long transmission line (TL) has to be used to transport the pulsed current to testing targets. The coaxial RG-218/U cables of characteristic impedance Z_o = 50 Ω are chosen as the TL for its power/current handling capabilities (maximum 11 kV)[5.A]. 8 parallel (to sustain high voltage applied from Marx bank) coaxial RG-218/U cables of 50 ft length with an inductance of 0.5 µH[5.A] is determined to connect the current generator to target load. Then the crucial load parameters for new DSLTF are much smaller, L_l = 0.5 µH ~1.0 µH (50 ft ~ 100 ft for 16 or 8 parallel RG-218/U) and R_s // R_l < 6mΩ (Figure 2.A), as compared to similar designs of British ABE's 8 µH, 10 mΩ[5.A] and SLS's old before refurbished 5.8 µH, 67 mΩ [1.A]. The lower load inductance make new DSLTF design very desirable and feasible for a compact portable system.

The RLC system design scheme without the crowbar switch of DSLTF at Redstone had been first under serious investigations. With given capacitances[5.A], the system parameters can be analytically solved for an overdamped condition from nonlinear couple equations by math tool MATHCAD for the *exact* double exponential direct strike waveform. This is performed along with all the calculations[5.A] of lower inductances from rectangular bus works for interconnections and grounding impedances. The design parameters can be iterated for the *exact* waveform for minimizing looping area (height *h*, length *l*) at the front end of TL. The optimized Marx generator would have capacitance 258 µF driven by DC power supply voltage of 74 kV and high energy shaping resistor of lumped 0.34 Ω. In the end, a spark gap dynamic resistance $R_{SG}(I_g, t)$ correlated to driven current I_g through Rompe and Weisel model[6] and breakdown criteria of (4`` brass ball, pneumatically driven) air gap with minimum separation d_{min} > 0.949 inches are incorporated to clarify the peak current and rise time. Neglect L_g, limit C_g of 206µF//52µF =258µF and V_g = 73.386 kV, system R = 0.347Ω it predicts R_{SG} dropped from 161.87 kΩ at t = 6.8 ns down to 25.7 mΩ at t > 161.7 ns[5.A], much faster as required.

The system design parameter surveys for required generator voltage V_g, system inductance L_g and pulse shaping resistance R, versus bank capacitance C_g, are concluded in Figure 1.

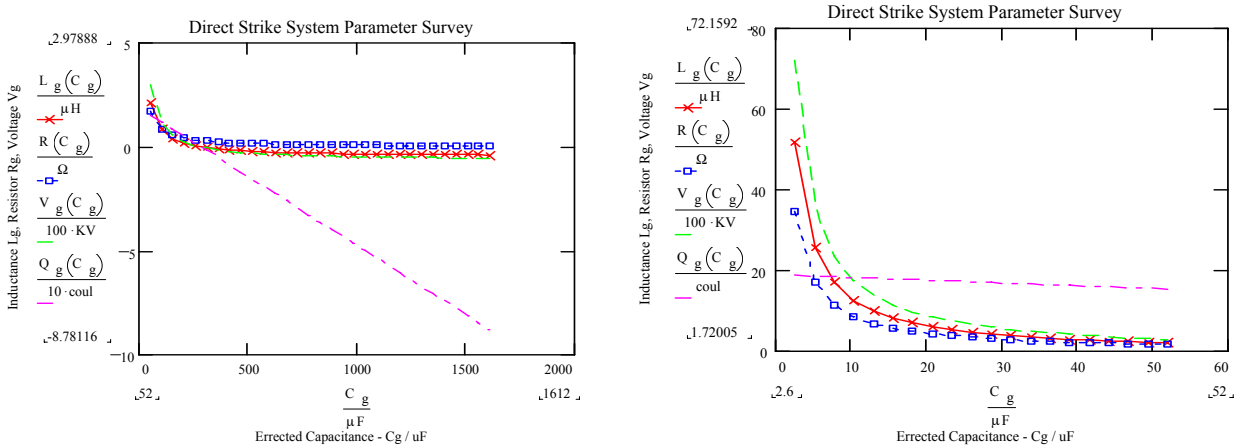

Figure 1. DSLTF Overdamped Parameter Surveys based on the off-shelf capacitor designs of G.A. Energy Products[5.B]. Note: *beyond 260 µF, the iterated L_g becomes negative and should not be considered, else reducing R-L_g-C_g loop (h, l) to impractical small size << 30" ×3".*

This information provides not only the clue for optimization but why conventional gigantic Mark generators require V_g of MV-scale for small C_g < 10 µF, and all these are driven by L_g. Regarding the desired energy deemed to furnish the charging action, it could require even higher capacitance of 206 µF up to 830 µF[5.A,B] (G.A. Energy Product #32349/#33593). It is demonstrated that the total action charge Q is near around

20 Coulombs slightly larger than MIL-STD required 18.87 Coulombs. However, it decreases to -8.78 Coulombs as L_g smaller than 0.047 μH to unacceptable negative at $C_g > 312$ μF[5.B], thus, dropped off as an option as further noted in Figure 1.

To relieve the severe constraint imposed by the system inductances of RLC circuitry to achieve an overall performance and small system size, it is genuinely thought of minimizing the net inductance by retaining inductances only *inherited* in the necessity TL, not inserting any inductor specially designed to overcome the extremely large e.m.f. force. Besides RG-218 TL, all the rest residual inductances[5.A] will be mostly resulted from the interconnections using parallel plates, sandwiched with Mylar to avoid voltage breakdown, with very narrow separation (feasible $h < 1$ cm) to significantly reduce the external inductances from loop area. Meanwhile, instead of regular spark gap, rail-gap switch of smaller inductance 20 nH is adopted to trigger parallel capacitors or mini-Marx bank to scale up the current.

As depicted with RLC formulae in Figure 2.A, the new simulator should act as an underdamped RLC circuit (or quasi-LC for negligible $R_s + R_{load} << [2L_T/C_g]^{1/2}$) so driving voltage and current have nearly 90° phase difference before the crowbar switch closes. Based on required zero-to-peak rise time 6.36 μs and $t_r = (1/\beta)\tan^{-1}\beta/\alpha \sim$ LC's quarter period $T/4 = \pi/2(L_T C_g)^{1/2}$, the desired capacitance C_g can be estimated for predetermined optimized system L_T[5.C] (excluding diodes) and iterated for refinement with spark gap dynamic resistance.

By taking advantage features of forward recovery process over reversed recovery process as described later, the diode set is initially *reverse* biased by the negative polarity of generator and automatically shunts the current pulse at the desired current peak point in time as discharging voltage changing its polarity to positive through quasi-LC oscillator bank– this is how diodes come to play as the essential role. While after crowbar switch closing the expected decay of load current I_{load}, damping in the closed RL sub-loop of load-TL-diode, should sustain by itself the pulse width t_{FWHM} (Full Width Half Maximum) of desired 68.0 μs (or 61.63 μs after peak time). The decay time constant is $(R_{on} + R_{load})/L_{load}$ where L_{load} is TL's inductance, R_{load} load resistance and R_{on} the dynamic resistance R_D of *conducting* diodes as described later in more details. The criteria $R_{on} << R_{load}$ is crucial for desired pulse width and associated charging action. This self-sustained scheme waives the load grounding issue.

To simplify the analysis, this crowbar circuitry is decoupled at $t > t_r$ rise time as diodes turn on, except Kirchhoff current law. The single RLC loop is divided into isolated branches of load-TL-diode and capacitor-resistor-R_g-diode. Vendor's I-V specifications are employed but extrapolated beyond specification $V_D > 9$V up to $V_{frm} \sim 3.26$ kV[3].

The optimized design data for erected capacitances are eventually determined as $C_g = 25$ μF of two parallel1 12.5 μF capacitors (G.A. Part # 32276) for the specified $L_{load} = L_{TL} = 0.5$ μH[5.C] at $V_g = -32$ kV.

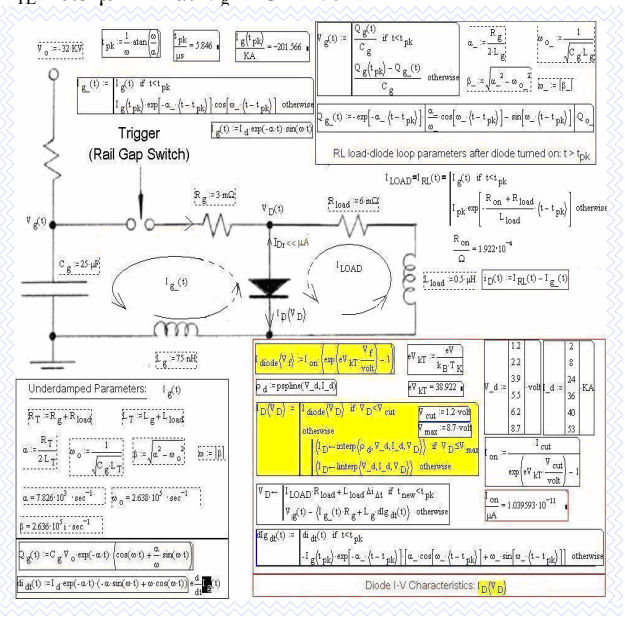

Figure 2.A MATHCAD Uncoupled Crowbar Circuit Model.

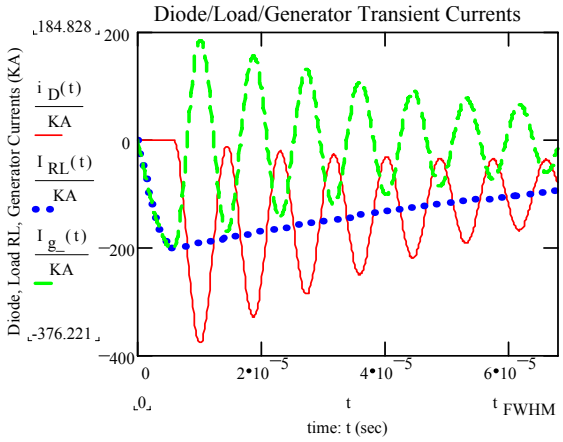

Figure 2.B MATHCAD Crowbar Circuit Simulations.

The results in Figure 2.B show how diode *forward* current $i_D < 0$ *oscillating* up to maximum $|i_D|$ 376 kA much higher than the required peak 200 kA of load current I_{RL}. This is due to the larger contributions from diode-capacitor branch of *under-damped oscillatory* condition with a significantly reduced sub-loop resistance as the diodes begin conducting. To accommodate it for diode maximum thermal rating this huge current must be distributed into more parallel sets of diodes, e.g., for an adopted Silicon Power # SDD303 of 100mm rectifier diode non-rep peak surge current 60 kA[3] at average 3.5 kA and threshold -6kV, to be conservative, it needs 6 (or lesser[3]) parallel files of 6 diodes stacked in each series to avoid breakdown.

IV. Pin Diode Forward Transient Simulations

Nomenclature in PiN Diode Characteristic Analysis -

P^+ - heavily-doped p-type region,
i - intrinsic region, or epilayer (subscript $_M$ for mid-region),
N^+ - heavily-doped n-type region,
(N_D, N_A) – (donor, acceptor) density (cm^{-3}),
N_B - background doping (cm^{-3}),
A - diode cross-sectional area (mm^2),
W - width of the i- middle (or s) layer: W = 2d (μm),
W_L is W normalized to L_d,
J_F - forward bias current density, I_F/A (A/mm^2),
(J_n, J_p) – (electron, hole) current density (A/mm^2),
n(x) or n(x, t), p(x) or p(x, t) – electron, hole density (cm^{-3}),
where $-d \le x \le +d$ - distance from P^+ edge toward N^+ edge,
t – time (ns.),
e - electron charge (C),
(D_n, D_P) – (electron, hole) diffusion coefficient (cm^2/s),
D_a - ambipolar diffusion coefficient (cm^2/s),
L_d - characteristic ambipolar diffusion length of injected charge carriers (μm),
τ - τ_{eff} carrier effective lifetime, τ_{hl} for high level injection ,
(μ_n, μ_p) – (electron, hole) mobility (cm^2/Vs),
δ - mobility deviation: $(\mu_n - \mu_p)/(\mu_n + \mu_p)$,
V_T – ($V_T = kT/e$) thermal voltage (V),
E(x) or E(x, t) - electric field defined in i-layer (V/cm),
V_P V_M V_N - voltage drops across P^+ (X = 0), i-, N^+ (X = W_L) layers (V)
V_D - diode voltage: $V_P + V_M + V_N = V_{PN} + V_M$, $V_{PN} = V_P + V_N$,
R_D - diode resistance (Ω or mΩ).

As PiN diode is switched on for *di/dt* > 0, the carriers in epilayer takes some time to reach the stationary flooded state, and the voltage drop at a given current will initially be higher. This effect, called forward recovery, results in a voltage overshoot and increasing dynamic losses.
Note: As the diode is turned off or oscillating in sinusoidal forms (as proposed design of under-damped capacitor-diode loop), it takes some time for carriers to recombine and to be extracted because the excess carriers in the epilayer cannot disappear immediately. So, the device is not able to reach the blocking state if carriers stored in the epilayer have not been extracted. This effect, called reverse recovery, results in the presence of a reverse current until the epilayer is free of excess carriers. It has unpleasant effects such as increase of dynamic losses (the current also flows through the switches used in the circuit, adding to power dissipation and degrading their reliability), electromagnetic interference (EMI), and limitation of maximum working frequency due to the *increased turn-off time*. Fortunately, in our design configurations, the diodes are first reverse biased and turned on forward subjected to *oscillating damping* (i_D in Figure 2.B)*, thus, without cross the zero voltage*, and this effect could be avoided.

PiN design parameters W, A, N_D, N_A and τ_{hl} are adjusted to comply with the peak diode current 376 kA along with the inclusions of breakdown voltage 6 kV criteria to emulate diode device design data which are extrapolated from existing data of 4 kV to 5 kV[7] voltage *breakdown resulted from impact ionizations*.

High level injection is assumed for high *di/dt* that

$N_D \sim n_o << \Delta n$, $N_A \sim p_o << \Delta p$,
hence $n \sim \Delta n \sim \Delta p \sim p$,

The diode physics can be interpreted by the Ambipolar Diffusion Equation (ADE)[7],

$$\partial n/\partial t = D_a \, \partial^2 n/\partial^2 x - n / \tau_{hl},$$
where $D_a = 2 D_n D_p / (D_n + D_p)$,
with Boundary Condition (B.C.): $\partial n/\partial x|_{x=-d} = - J_F / 2eD_p$
$\partial n/\partial x|_{x=+d} = - J_F / 2eD_n$
Initial Condition (I.C.): $n(x, t=0) \approx p(x, t=0) = 0$.
(where I.C. is only applicable to transient case)

And the transient solution in normalized X, T is [5.D, 8]

$$p(X, T) = (J_F L_d / 2 eW_L D_p D_n) \{(D_{p+} D_n)(1 - e^{-T}) + 2 \Sigma_{n\ge1}(-1)^n \{[1 - \exp\langle -T[(n\pi/W_L)^2 +1]\rangle / [(n\pi/W_L)^2 +1]\} [D_n \cos(n\pi\langle(x/W_L) -1\rangle) + D_p \cos(n\pi\, x/W_L)]\}$$

where $0 \le X \le W_L$ is x normalized to L_d,
T – time t normalized to τ.

and diode voltage $V_D(T) = V_P(T) + V_M(T) + V_N(T)$
where

$$V_M(T) := \frac{J_F(T)\cdot L_d}{e\cdot(\mu_n+\mu_p)}\cdot\int_{-\frac{W_L}{2}}^{W_L}\frac{1}{n(X,T)}\,dX - \delta\cdot V_T\cdot\ln\left[\frac{n\left(\frac{W_L}{2},T\right)}{n\left(-\frac{W_L}{2},T\right)}\right]$$

$$V_P(T) := V_T\cdot\ln\left(\frac{n(0,T)\cdot N_D}{n_i^2}\right), \qquad V_N(T) := V_T\cdot\ln\left(\frac{n\left(W_L,T\right)}{N_D}\right)$$

While the Steady State(S.S.) solution ($\partial n/\partial t \equiv 0$)) is [5.D]

$$V_M := 2\cdot\frac{L_d}{\tau_{hl}\cdot(\mu_n+\mu_p)}\cdot\int_{-d}^{d}\frac{1}{I(x)}\,dx - \delta\cdot V_T\cdot\ln\left(\frac{I(d)}{I(-d)}\right),$$

where

$$I(x) := \frac{\cosh\left(\frac{x}{L_d}\right)}{\sinh\left(\frac{d}{L_d}\right)} - \delta\cdot\frac{\sinh\left(\frac{x}{L_d}\right)}{\cosh\left(\frac{d}{L_d}\right)}.$$

S.S. approach predicts PiN diode resistance[5.D] $R_D \sim 0.008913$ mΩ well agree with transient's 0.009008 mΩ at peak diode current of 376 kA, amazingly small enough (as compared to specification 0.1922 mΩ for $I_D < 60$ kA in Figure 4.A) to sustain desired longer pulse decay. However, these simulations might improperly extrapolate V_D beyond 4 volts to few kV, due to imbedded *saturation* effect of so-called *conductivity modulation*. Note that in each transient step the solutions are derived from Laplace transform by artificially forcing current density J_F constant, i.e., *di/dt* = 0, so V_D just oscillating (not overshooting) exactly sinusoidal as fed from the generator underdamped current I_g ringing in RLC sub-loop as manifested in Figure 2.B. Thus, it would not furnish the overshoot driving mechanism to the diode forward

recovery voltage V_{frm} vs *di/dt*, as reflected in the specifications, Figure 4.A.

In addition, the electrical field built in by carrier profile is [5D, 6]

$$E_M(X,T) := \frac{J_e(T)}{n(X,T)} - \frac{\delta}{n(X,T)} \cdot \frac{d}{dX} n(X,T)$$

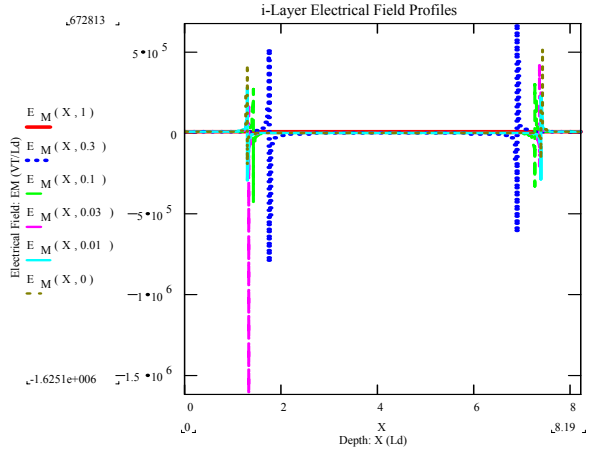

Figure 3. Field Spikes in Diode Forward Recovery Processes

Note: *Fields in epilayer E_M are functions of normalized X, T. E_{Mmax} ~ +672.8 kV/m to –1.625 MV/m, while avalanche breakdown in Silicon[7] is $E_{br}(N)$ ~ 0.2 ~ 0.4 MV/m for dopant concentration N = 10^{14} ~ 10^{16} cm^{-3} (c.f. in air E_{br} ~ 2.66 MV/m).*

As shown in Figure 3, the fields oscillate within some narrow regions of the epilayer with few spikes during the transient forward recovery process. It is caused by the uneven distributions of carrier profile, i.e., sharp change in dn(x, t)/dx as *evolved along with time t* regardless of the *ideal* neutrality assumption. This definitely would have impact on the diode reliabilities and life expectations once the spikes exceed the field breakdown. It is still subjected to more accurate realistic numerical modeling, including *di/dt* and other feedback effects.

The transient models of I-V (1st half cycle) and max forward recovery voltage V_{frm} vs *di/dt* are compared with the specifications
from Silicon Power in Figures 4.B and 4.A, respectively. Silicon Power claimed unable to predict or provide any verified I-V or R_D correlations for range much higher beyond 9 volts to few tens kV due to incapable measurement technologies. Mr. Dante Piccone from Silicon Power[3] had hand calculations for diode V_{frm} exceeding the range in data sheet estimated up to 3 kV with decay time t_{fr} around 3 µs, but just cannot afford sophisticated code for diffusion physics computations for higher kV range, thus, it relies on our own sake.

It shows in Figure 4.B that the envelops or saturated values of analytically simulated V_{frm} (*di/dt*) correlation are similar to the specifications except drastic oscillations displayed. The specification data might be measured statistically in static mode, thus incapable to differentiate the transient time T dependent oscillating disturbances.

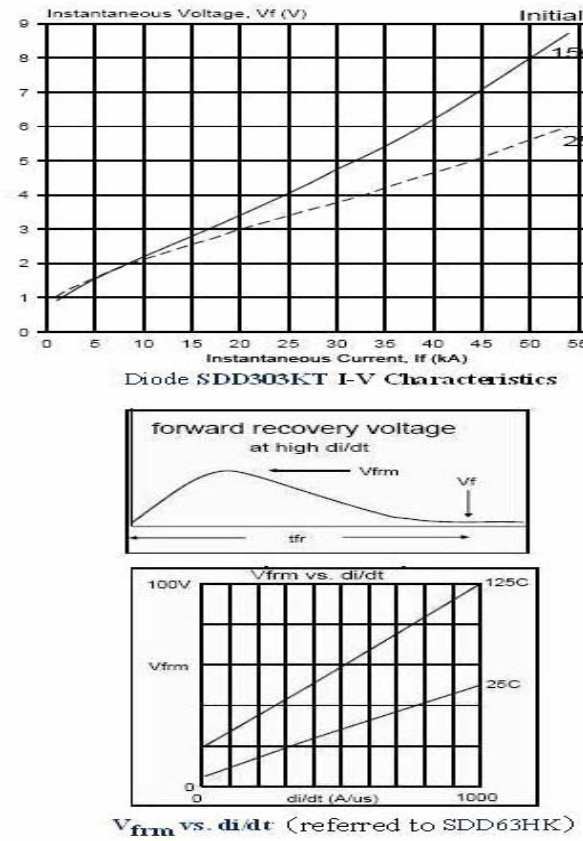

Figure 4.A Specifications from Silicon Power, Inc.

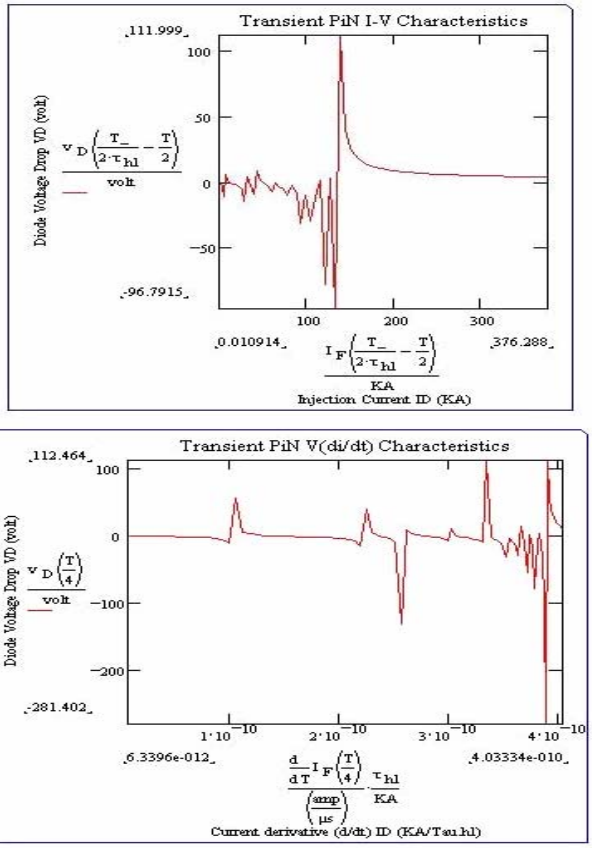

Figure 4.B MATHCAD Simulations for Transient I-V Characteristics and V_{frm} vs *di/dt*.

Around I_F > 120 kA, transient V(I) correlation, however, has diode voltage amplitude V_D over 112 volts, 6.2 times larger than that extrapolated from specifications at 25°C, 2×6= 18 volts. It may be exaggerated by the high level injection and transient disturbances in carrier distributions. All these are subject to further clarifications over delicate diode physics mechanisms as described below.

V. Power Diode Physics and Clarifications of Various Effects

Besides that the physics and geometry parameters of doping concentrations, layer width should not be constant through doped P^+ and N^+ regions and the Laplace transform for transient solutions assuming zero *di/dt* is never manifested properly in conductivity modulation according to carriers distribution. There are more delicate physics mechanisms involved in the epilayer should be considered:

* electron/hole mobilities - decrease for higher diode temperature and impurity concentrations, all time-space dependence and varied with spatial carriers profiles;
* carrier drift velocities - increase as induced fields E increase, and saturated after E > MV/m to 10 MV/m;
* recombination effect – minority carrier lifetime decreases rapidly with increasing doping level at P^+ and N^+ end regions, contribute to more forward current;
* Bandgap narrowing effect – caused by impurity band formation and band tailing and screening for high doping levels, the intrinsic carrier concentration arises accordingly;
* conductivity modulation reduction – increase resistivity due to
  - Carrier-carrier scattering increases for higher (injected) current, causing reduction in diffusion length
  - Auger recombination increases in end regions for injection higher, reduce carrier lifetime.

Any effects described above causing the *increase of the (mostly epilayer) resistivity* have *adverse impact* on diode performance in the whole system design, thus requiring further investigations.

And realistic theoretical methods involving

* Poisson's, continuity and ADE or even transport equations - only be solvable numerically by variation perturbation methods
* feedback from coupled two sub-loops circuitry, a correlation of load current $I_{load}(t)$ to diode resistance $R_D(t)$ can be derived as [5.A].

$$I_{load}(t) = [R_D(t) / (R_{load} + R_D(t))] \; [\int_o^t dt \, (V_g / L_g) \exp\{\int_o^t dt \; R_D(t) \, R_{load} / L_g \, (R_{load} + R_D(t))\} + Ig(t=0)] * \exp\{\int_o^t dt \; R_D(t) \, R_{load} / L_g \, (R_{load} + R_D(t))\}.$$

This nonlinear feedback mechanism, incorporated into advanced diffusion physics model to form a complete realistic system of equations, should be able to properly simulate the carriers behavior – a large scale complicated FORTRAN 1-D transient code of finite difference numerical algorithms running on High Performance Computer, or supercomputer if necessary, is undergoing an elaborate implementation. Eventually it would accurately predict transient I-V Characteristics to full extent operating voltages so as to resolve the technical issues for *di/dt*, modulation conductivity and associated higher fields and carriers effects on diode dynamic temperature dependent resistance, overshoot and reduction on pulsed width.

It should be pointed out that the complete realistic physics model is essential to clarify the higher conductivity modulation and sort out possibly inherited self-healing mechanisms. If so, it might reduce the diode peak current 376 kA based on decoupled RLC circuitry with improper *extrapolation* of *non-saturated* diode I-V characteristics, also, to smooth out the erratic transient behaviors and breakdown constraints – all these would significantly cut down the total number of diodes without degradation on operation performance. On the contrary, if the realistic physics model would indicate even worst results from the impact of oscillating in even higher diode currents or voltages, then more diodes would be required in each series and parallel sets along with effective cooling; else it would be deemed to enhance diode structure designs and doping concentrations and profiles: or worst, the underdamped diode-capacitor configuration might necessarily be modified to overdamped configuration ending up with larger system resistances R, in turn, require to increase the crucial system inductances L_g, inevitable higher cost bank voltage V_g (see Figure 1) to provide the desired peak current, in order to accommodate the impact on current pulse peak time due to significantly out of 90° phase shifting in driven voltage and current.

V. CONCLUSIONS

After exhaustive examinations over various design approaches and methodologies, it shows the high-power diodes as crowbar switch for new DSLTF has tremendous cost saving with total hardware material costs less than $70 K. It is a very compact portable design of only couple capacitors driven by very low DC supply without the needs of insulation oil and any external electronic controlled triggering as compared to all other known existing DSLTFs.

Analytical models can plausibly predict the *saturated* diode dynamic resistance but incapable to simulate the overshoot of V_D during the Forward or Reverse Recovery Transient processes for $di/dt \neq 0$. This can be remedied by the numerical simulations through more realistic coupled nonlinear circuitry along with the accurate device physics to resolve the high *di/dt* involved overshoot problems, effects on pulse width and diode thermal impendence impact on crowbar switch operation.

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[2] Dr. Charles R. McClenahan, High Power Consulting, Inc.

[3] Dante Piccone, Silicon Power, Inc.

note: the peak surge current i_D ~ 60 kA measured at 9 volts, it could be much larger at higher (or overshoot) max forward recovery voltage V_{frm} ~ 3 kV.

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Table 1. Design Options and Cost Estimations of System Components for Lightning Test Facility[5.A]

WSMR Proposed Lightning Test Facility (LTF) based on **Inductive Energy Storage Pulsing System** employing Opening Switch (OS)					
Manufacturer	Part Number	Descriptions	Unit Costs $	Quantity Required	Delivery Schedule weeks ARO
General Atomic	CCS12015P10	12kJ/sec., 15kV, instrumented power supply with positive output and 480vac, 3ø input	$14,220	1	10 ~ 12
	32327	830 uF, 11 kV capacitor 12.0 x 16.0 x 27.5"	$8,760	2	18
	32283	52 uF, 44 kV capacitor 12.0 x 16.0 x 27.6"	$9,820	1	18
L-3 Communications	50-0249-202	T-150 Spark Gap (Close Switch)	$4,450	2*	3
(Titan)	ST-300B	ST-300B, 0-55 kV, 600 kA (Close Switch)	$4,894	2*	16
High Power Consulting		exploding foil fuses Opening Switch (OS - full interruption infinite off resistance)	$10,000	1	2 ~ 4
Stangenes Industries		Inductor of 2.45 uH (inductance subjected to final tuning ? $2 K ~ $4K)	$4,000	1*	
WSMR stock?		RG-218 Coaxial cable (interchangeable with parallel plate Transmission Line below)		8 ~ 10	
Unknown (Titan ?)		parallel plate Transmission Line about 100 ft sandwiched with Mylar	$35	100	
Unknown (or WSMR stock?)		Bus work or bus bar			
		Total estimated proposed WSMR direct strike simulator - (see Comments)	$66,844		
Close Switch (CS) Alternations ---		**major CS for Capacitive Energy Storage Pulsing System**			
ABB Switzerland Ltd	5SPY 36L4506	Reverse Blocking Capacitor Discharge Switch Assembly: 20 kvdc, Ipk:200 kA	$167,000	2 x 32	
OptiSwitch Tech., Corp	new	thyristor based solid state CS: Pulse current 80 kA (with laser trigger @ $20 K)	$10,000	3 x 2	
(Ignitron or Thyratron)		might be applicable, but no specifications or market pricing being searched yet	?		
Silicon Power, Inc.	SDD303	100mm rectifier diode Non-rep peak surge current 60 kA @ Average 3.5 kA	$1,200	6	> 12
Silicon Power, Inc.	Super-GTO	4 parallel module discharge @ 9 m-ohm, 575nH - Di/dt ~ 200kA/ µs, I_{pk}>200kA	> $65 K?	2x8-die	
Opening Switch (OS) Alternations ---					
L-3 Communications	TG70	Plasma Erosion Opening Switch (max off resistance ~ 10 Ohms only, more studies needed)	$100,000	1	4 ~ 8
USC -Martin Gundersen		Pseudospark Switch - capable for both functions of closing and opening switch - but asking 18 months @ $250k for the first year, $150k for the next 6 months for OS R&D design	> $250k	1	18
HTM Technologies		explosive wire Opening Switch	$30 K~$50 K	1	
Institute of Electrophysics		Semiconductor Opening Switch (SOS) interruption @ 32kA at 200kV	$200 K	6 ~ 7	
(Photoconductive OS)		might be applicable, but requiring R&D to enhance sustaining current with longer laser wavelengths			
Cost Comparisons with other Lightning Test Facilities (all indirect strike except direct strike made by Redstone)					
	Applications	(All based on **Capacitive Energy Storage Pulsing System**, i.e., using **conventional Mark Generator** except Resonance Research's)			
Resonance Research, Inc's proposal	indirect strike	Simulator for all components A, B, C, D, D/2 and H - LC resonators with **chopper** technologies without Mark Generator	$ 250K	initial design	@ $16 K
Redstopne simulator	direct strike	conventional double exponential overdamped RLC circuitry	?		
Sandia simulator	indirect strike #	- crowsbar switch (to replace peaking capacitor) with YAG laser trigger	> $250 K ?		
BAE simulator	indirect strike #	- crowbar switch	> $1 M		
Panx River simulator	indirect strike	- peaking capacitor (similar to WSMR)	>> $1 M		
WSMR	indirect strike #	- peaking capacitor, originally designed by Thiokol for NASA:	free except shipping and parts replace		
These are alternate parts for items in previous rows at similar prices					
These highlighted costs are not formally quoted but with oral estimations from designers or vendors					
These highlighted costs are not quoted yet, just a guess.					